S03P1171仮図面

FIG. 1A

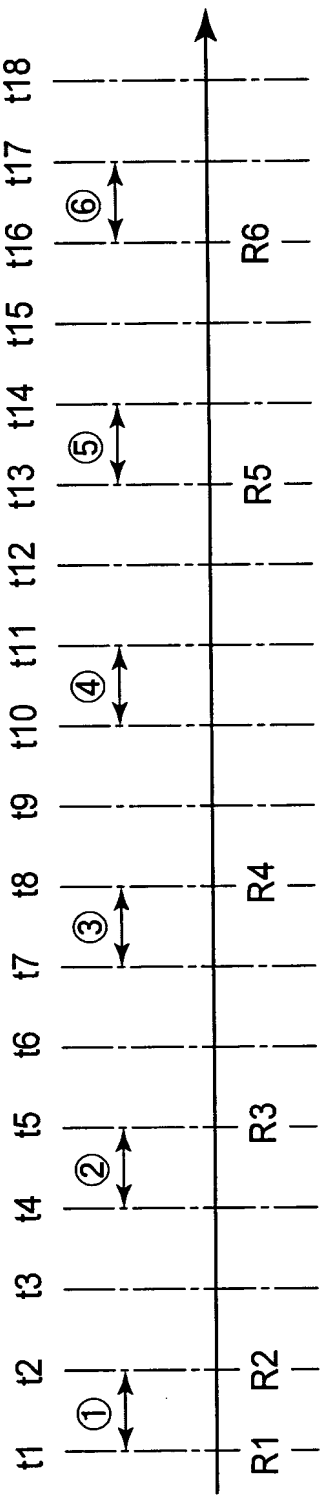


FIG. 1B

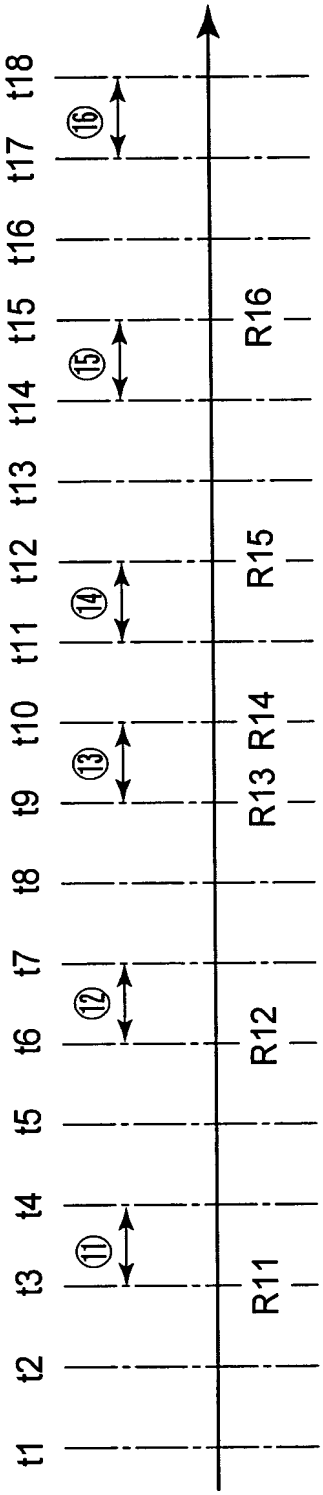


FIG. 2

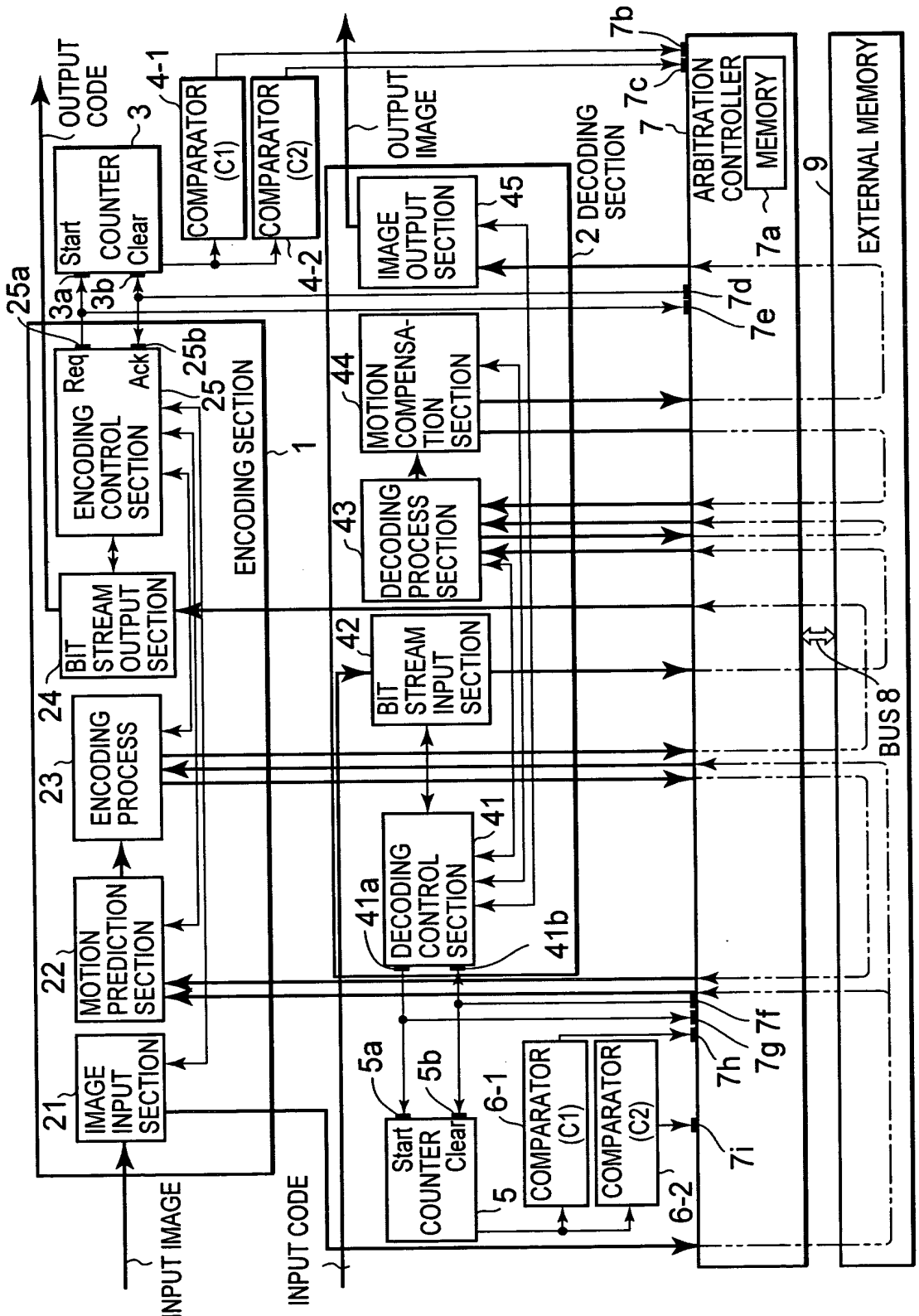

INPUT IMAGE
INPUT CODE
OUTPUT CODE
OUTPUT IMAGE
EXTERNAL MEMORY
BUS 8
ENCODING SECTION
1
2 DECODING SECTION
IMAGE INPUT SECTION
21
MOTION PREDICTION SECTION
22
ENCODING PROCESS
23
BIT STREAM OUTPUT SECTION
24
ENCODING CONTROL SECTION
25
Req
Ack
25a
25b
COUNTER
Start
Clear
3
3a
3b
COMPARATOR (C1)
COMPARATOR (C2)
4-1
4-2
BIT STREAM INPUT SECTION
42
DECODING PROCESS SECTION
43
MOTION COMPENSATION SECTION
44
IMAGE OUTPUT SECTION
45
DECODING CONTROL SECTION
41
41a
41b
5
5a
5b
6-1
6-2
7
7a
7b
7c
7d
7e
7f
7g
7h
7i
ARBITRATION CONTROLLER
MEMORY
9

FIG. 3

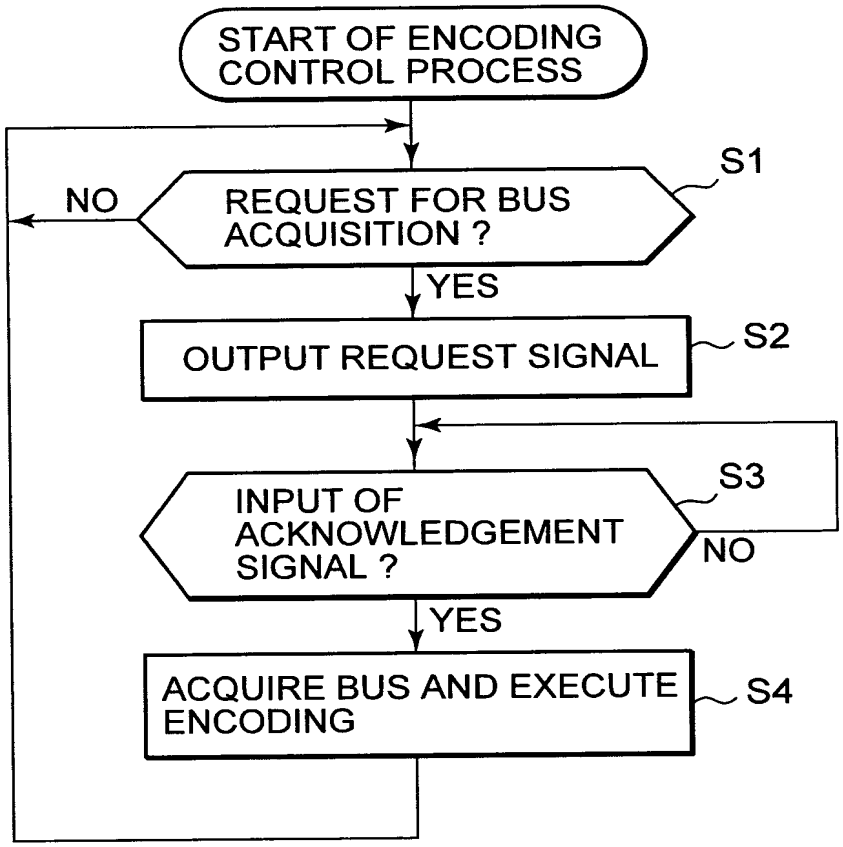

START OF ENCODING CONTROL PROCESS
S1
NO
REQUEST FOR BUS ACQUISITION ?
YES
OUTPUT REQUEST SIGNAL
S2
S3
INPUT OF ACKNOWLEDGEMENT SIGNAL ?
NO
YES
ACQUIRE BUS AND EXECUTE ENCODING
S4

FIG. 4

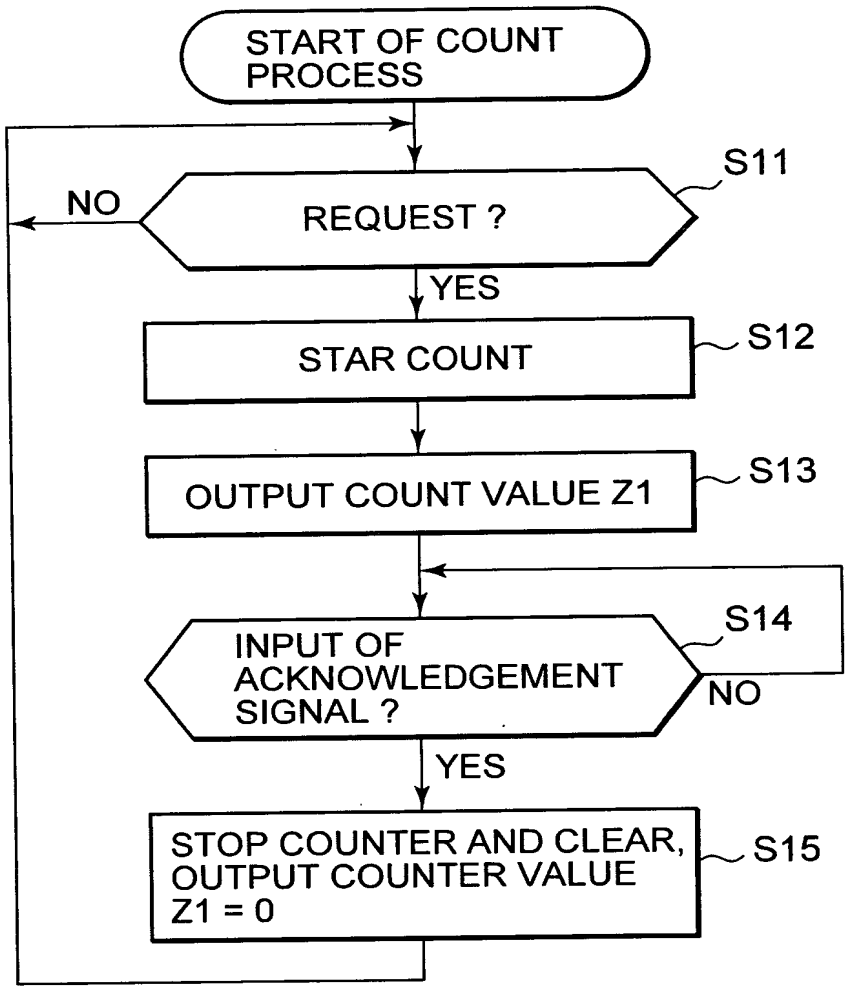

START OF COUNT PROCESS
S11
REQUEST ?
NO
YES
S12
STAR COUNT
S13
OUTPUT COUNT VALUE Z1
S14
INPUT OF ACKNOWLEDGEMENT SIGNAL ?
NO
YES
STOP COUNTER AND CLEAR, OUTPUT COUNTER VALUE Z1 = 0
S15

FIG. 5

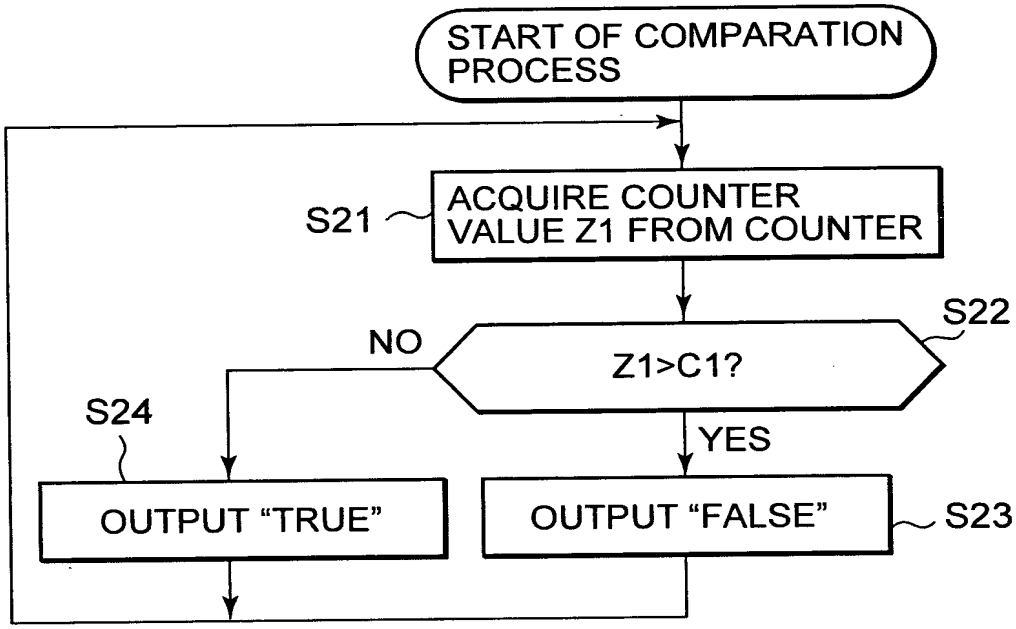

START OF COMPARATION PROCESS
S21
ACQUIRE COUNTER VALUE Z1 FROM COUNTER
S22
NO
Z1>C1?
YES
S24
OUTPUT "TRUE"
OUTPUT "FALSE"
S23

FIG. 6

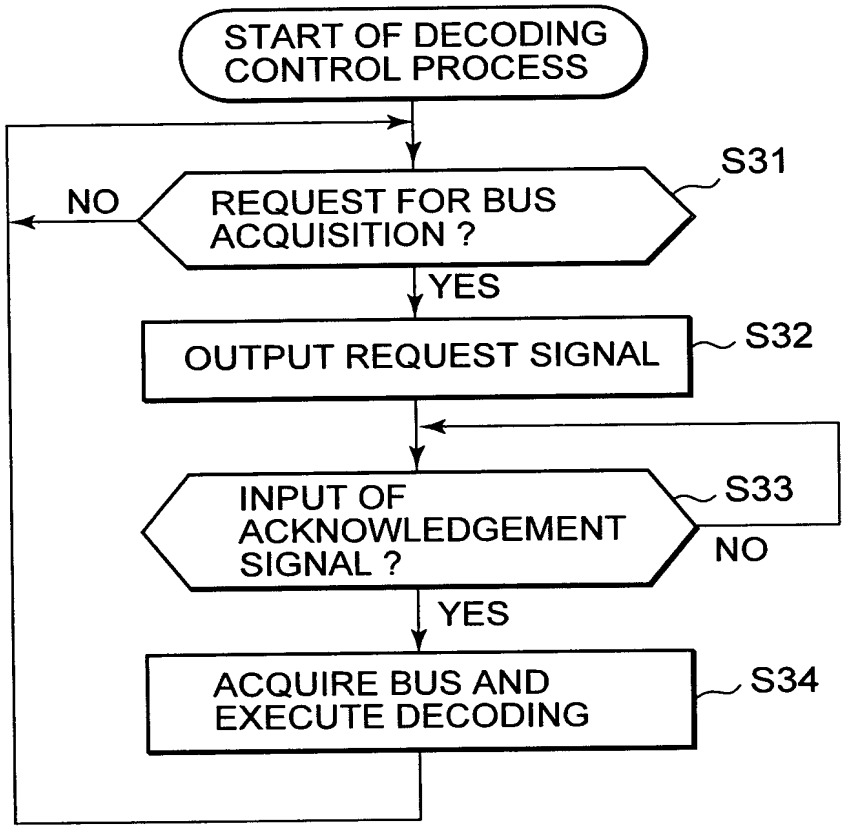

START OF DECODING CONTROL PROCESS
S31
NO
REQUEST FOR BUS ACQUISITION ?
YES
OUTPUT REQUEST SIGNAL
S32
INPUT OF ACKNOWLEDGEMENT SIGNAL ?
S33
NO
YES
ACQUIRE BUS AND EXECUTE DECODING
S34

FIG. 7

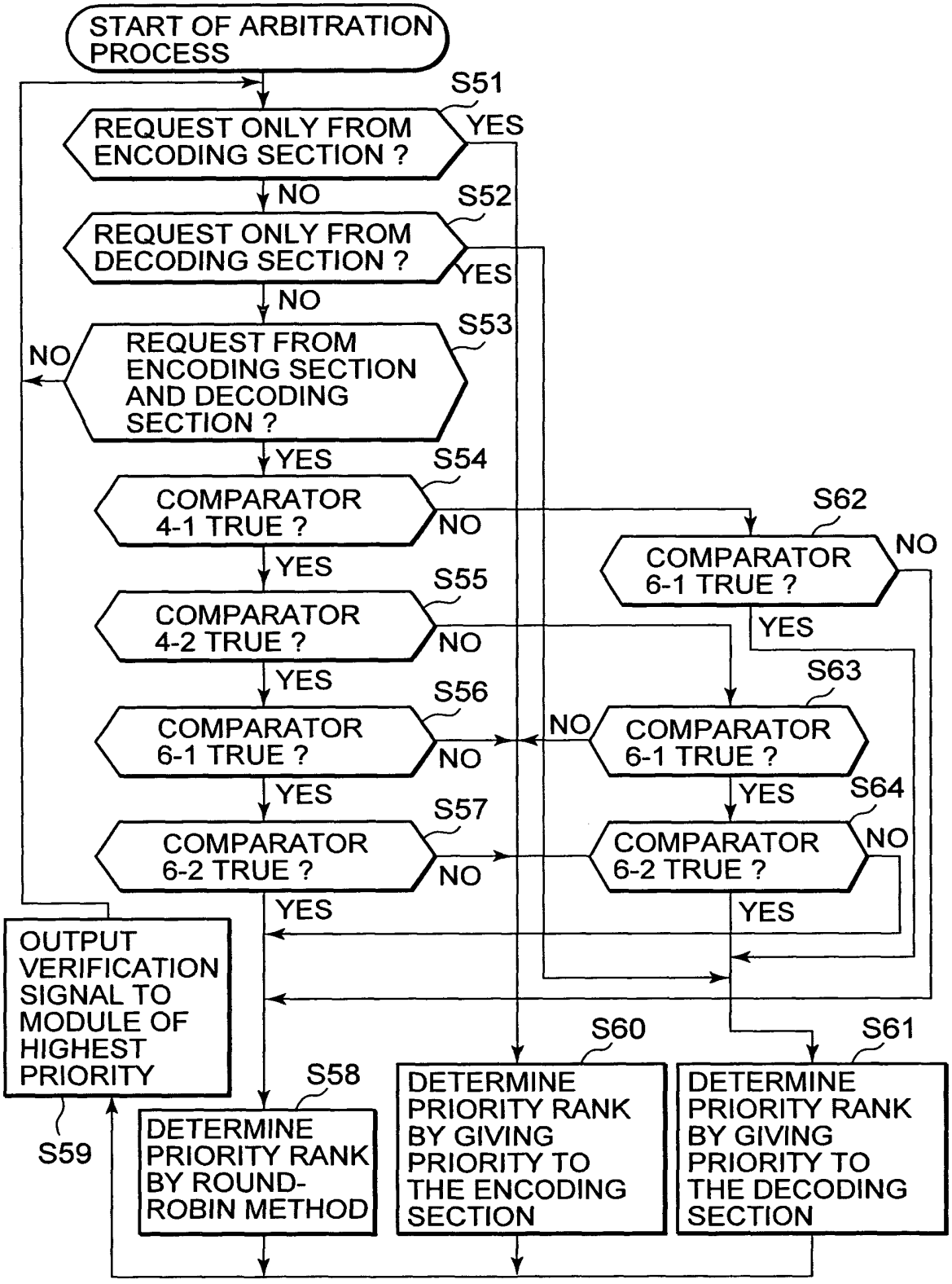

START OF ARBITRATION PROCESS
S51
REQUEST ONLY FROM ENCODING SECTION ?
YES
NO
S52
REQUEST ONLY FROM DECODING SECTION ?
YES
NO
S53
REQUEST FROM ENCODING SECTION AND DECODING SECTION ?
NO
YES
S54
COMPARATOR 4-1 TRUE ?
NO
YES
S55
COMPARATOR 4-2 TRUE ?
NO
YES
S56
COMPARATOR 6-1 TRUE ?
NO
YES
S57
COMPARATOR 6-2 TRUE ?
NO
YES
S62
COMPARATOR 6-1 TRUE ?
NO
YES
S63
COMPARATOR 6-1 TRUE ?
NO
YES
S64
COMPARATOR 6-2 TRUE ?
NO
YES
OUTPUT VERIFICATION SIGNAL TO MODULE OF HIGHEST PRIORITY
S59
S58
DETERMINE PRIORITY RANK BY ROUND-ROBIN METHOD
S60
DETERMINE PRIORITY RANK BY GIVING PRIORITY TO THE ENCODING SECTION
S61
DETERMINE PRIORITY RANK BY GIVING PRIORITY TO THE DECODING SECTION

FIG. 8A

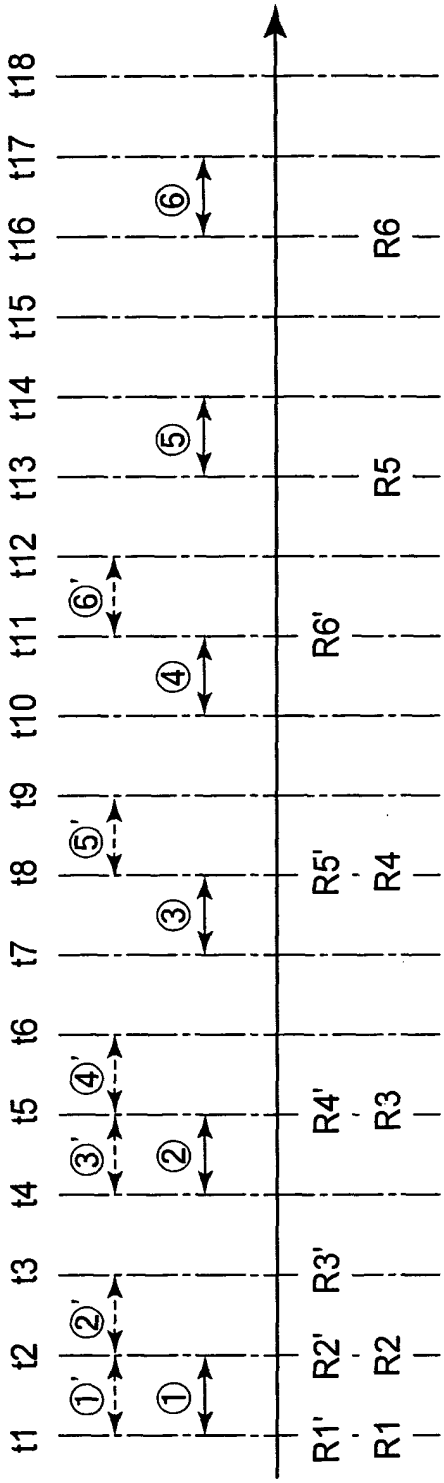

t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16 t17 t18
①' ② ②' ③ ③' ④ ④' ⑤ ⑤' ⑥ ⑥'
R1' R1 R2' R2 R3' R3 R4' R4 R5' R5 R6' R6

FIG. 8B

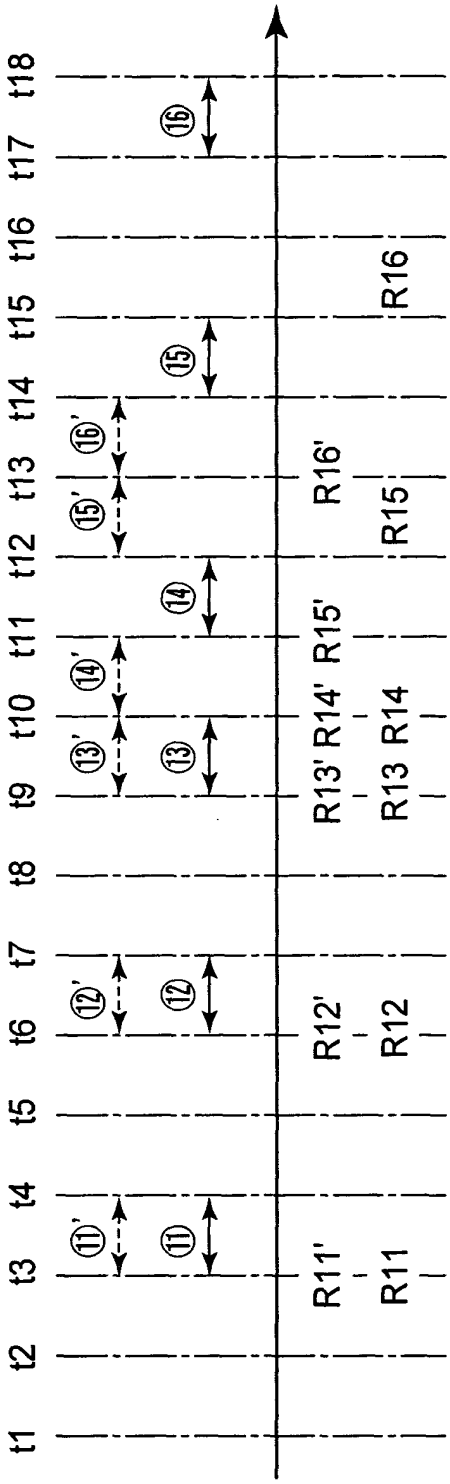

t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16 t17 t18
⑪' ⑪ ⑫' ⑫ ⑬' ⑬ ⑭' ⑭ ⑮' ⑮ ⑯' ⑯
R11' R11 R12' R12 R13' R13 R14' R14 R15' R15 R16' R16

FIG. 9

	ENCODING SECTION (M0)		DECODING SECTION (M1)	
	Comp4-1	Comp4-2	Comp6-1	Comp6-2
R(M0,M1)	0	0	0	0
	1	0	1	0
	1	1	1	1
M0,M1	1	0	0	0
	1	1	0	0
	1	1	1	0
M1,M0	1	0	1	1
	0	0	1	1
	0	0	1	0

FIG. 10

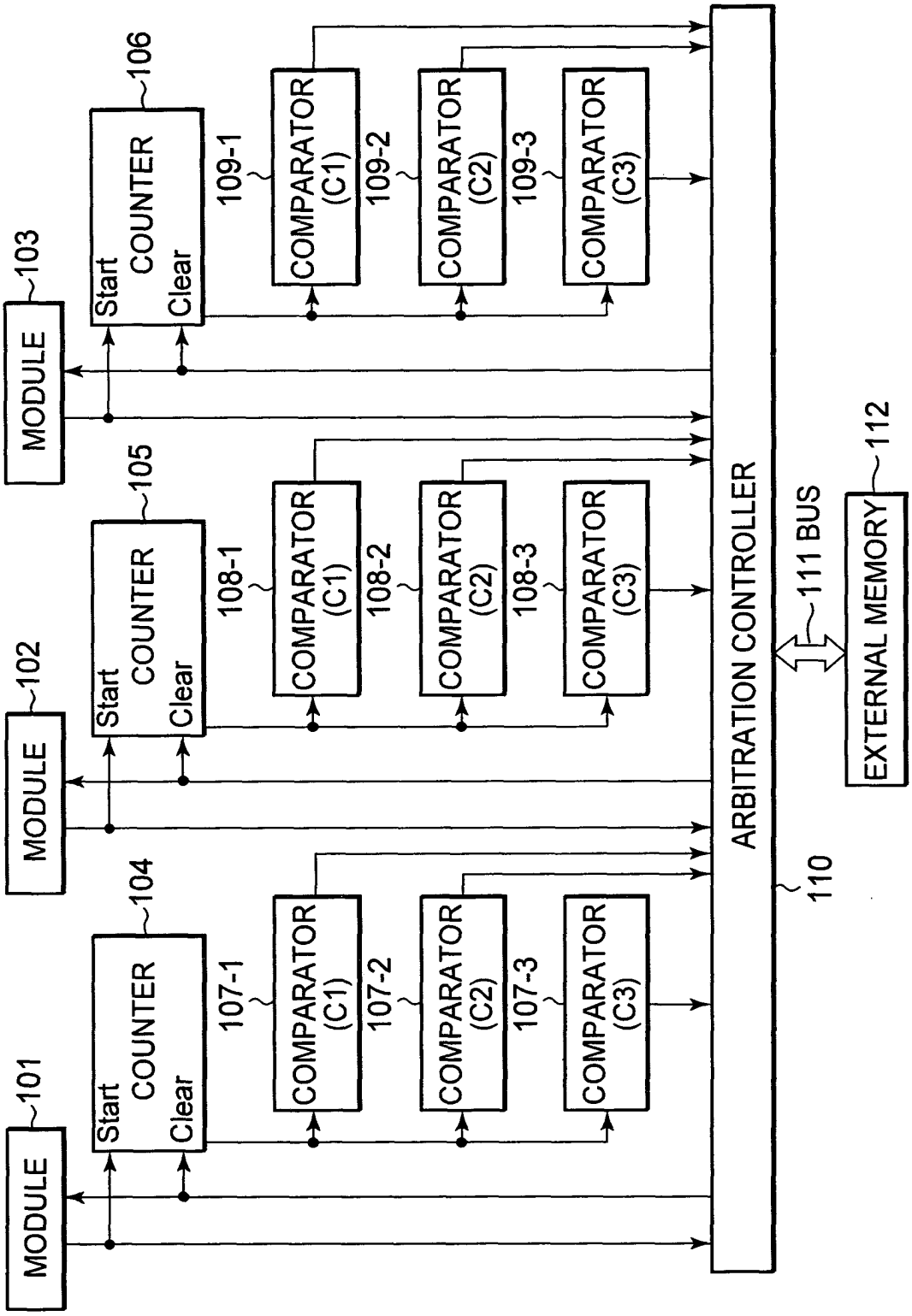

MODULE
101
MODULE
102
MODULE
103
Start
COUNTER
Clear
104
Start
COUNTER
Clear
105
Start
COUNTER
Clear
106
107-1
COMPARATOR (C1)
107-2
COMPARATOR (C2)
107-3
COMPARATOR (C3)
108-1
COMPARATOR (C1)
108-2
COMPARATOR (C2)
108-3
COMPARATOR (C3)
109-1
COMPARATOR (C1)
109-2
COMPARATOR (C2)
109-3
COMPARATOR (C3)
ARBITRATION CONTROLLER
110
111 BUS
EXTERNAL MEMORY
112

FIG. 11

	M0			M1			M2		
	Comp107-1	Comp107-2	Comp107-3	Comp108-1	Comp108-2	Comp108-3	Comp109-1	Comp109-2	Comp109-3
R(M0,M1,M2)	0	0	0	0	0	0	0	0	0
	1	0	0	1	0	0	1	0	0
	1	1	0	1	1	0	1	1	0
	1	1	1	1	1	1	1	1	1
M0,R(M1,M2)	1	0	0	0	0	0	0	0	0
	1	1	0	0	0	0	0	0	0
	1	1	0	1	0	0	1	0	0
	1	1	1	0	0	0	0	0	0
	1	1	1	1	0	0	1	0	0
	1	1	1	1	1	0	1	1	0
R(M1,M2)M0	0	0	0	1	0	0	1	0	0
	0	0	0	1	1	0	1	1	0
	0	0	0	1	1	1	1	1	1
	1	0	0	1	1	0	1	1	0
	1	0	0	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	1
M0,M1,M2	1	1	0	1	0	0	0	0	0
	1	1	1	1	0	0	0	0	0
	1	1	1	1	1	0	0	0	0
	1	1	1	1	1	0	1	0	0
M0,M2,M1	1	1	0	0	0	0	1	0	0
	1	1	1	0	0	0	1	0	0
	1	1	1	0	0	0	1	1	0
	1	1	1	1	0	0	1	1	0

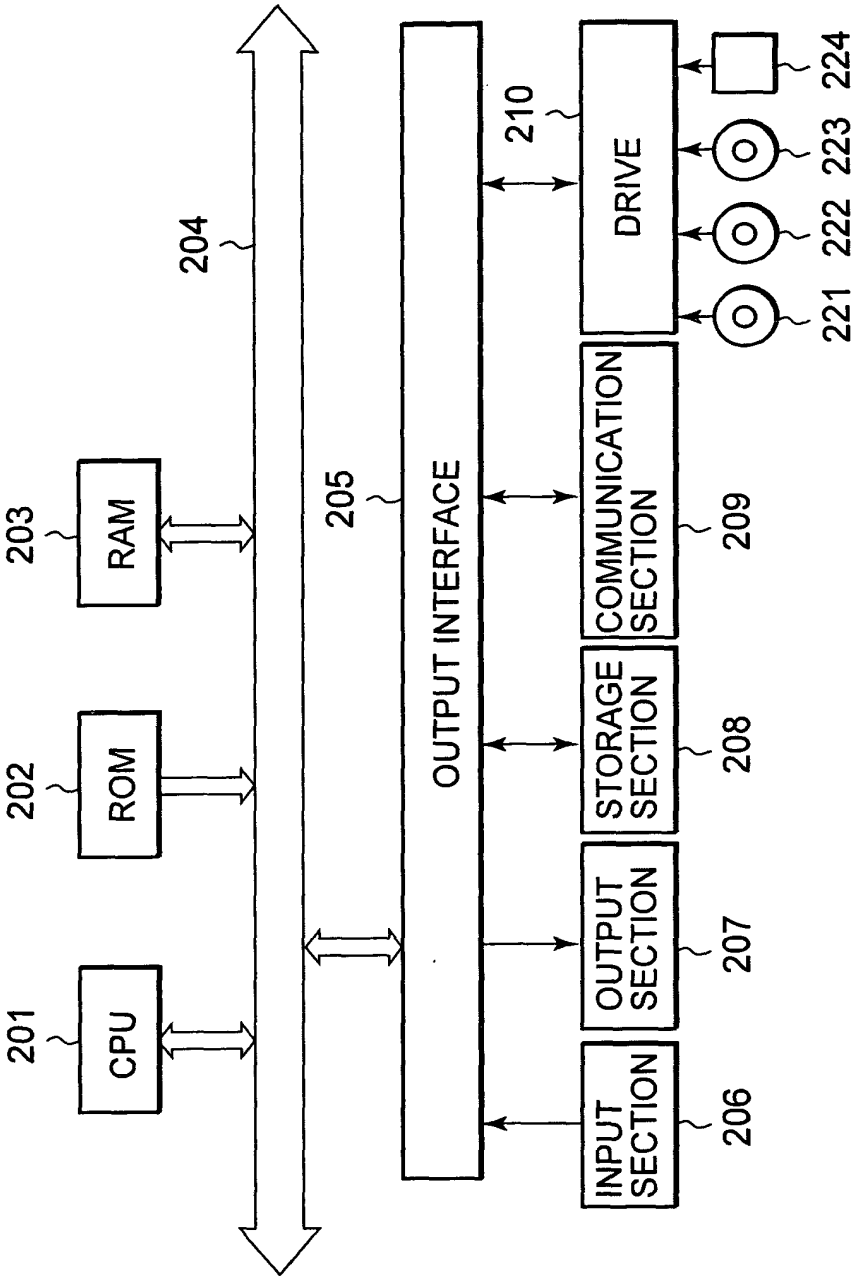
FIG. 12

	M0			M1			M2		
	Comp107-1	Comp107-2	Comp107-3	Comp108-1	Comp108-2	Comp108-3	Comp109-1	Comp109-2	Comp109-3
M1,R(M0,M2)	0	0	0	1	0	0	0	0	0
	0	0	0	1	1	0	0	0	0
	1	0	0	1	1	0	1	0	0
	0	0	0	1	1	1	0	0	0
	1	0	0	1	1	1	1	0	0
	1	1	0	1	1	1	1	1	0
R(M0,M2),M1	1	0	0	0	0	0	1	0	0
	1	1	0	0	0	0	1	1	0
	1	1	1	0	0	0	1	1	1
	1	1	0	1	0	0	1	1	0
	1	1	1	1	0	0	1	1	1
	1	1	1	1	1	0	1	1	1
M1,M0,M2	1	0	0	1	1	0	0	0	0
	1	0	0	1	1	1	0	0	0
	1	1	0	1	1	1	0	0	0
	1	1	0	1	1	1	1	0	0
M1,M2,M0	0	0	0	1	1	0	1	0	0
	0	0	0	1	1	1	1	0	0
	0	0	0	1	1	1	1	1	0
	1	0	0	1	1	1	1	1	0

FIG. 13

	M0			M1			M2		
	Comp107-1	Comp107-2	Comp107-3	Comp108-1	Comp108-2	Comp108-3	Comp109-1	Comp109-2	Comp109-3
M2,R(M0,M1)	0	0	0	1	0	0	1	0	0
	0	0	0	1	0	0	1	1	0
	1	0	0	1	0	0	1	1	0
	0	0	0	0	0	0	1	1	1
	1	0	0	1	0	0	1	1	1
	1	1	0	1	1	0	1	1	1
R(M0,M1),M2	1	0	0	1	0	0	0	0	0
	1	1	0	1	1	0	0	0	0
	1	1	1	1	1	1	0	0	0
	1	1	0	1	1	0	1	0	0
	1	1	1	1	1	1	1	0	0
	1	1	1	1	1	1	1	1	0
M2,M0,M1	1	0	0	0	0	0	1	1	0
	1	0	0	0	0	0	1	1	1
	1	1	0	0	0	0	1	1	1
	1	1	0	1	0	0	1	1	1
M2,M1,M0	0	0	0	1	0	0	1	1	0
	0	0	0	1	0	0	1	1	1
	1	0	0	1	1	0	1	1	1
	0	0	0	1	1	0	1	1	1

FIG. 14


201
CPU
202
ROM
203
RAM
204
205
OUTPUT INTERFACE
206
INPUT SECTION
207
OUTPUT SECTION
208
STORAGE SECTION
209
COMMUNICATION SECTION
210
DRIVE
221
222
223
224